FPGAtors

FALL 2026

General Body Meeting 2

09/30/2026 • LAR 234

Scan for attendance

Recap on FPGAtors

- FPGAtors is a pre-professional organization for UF ECE students building a career in hardware design and verification.
- FPGAtors is a group of enthusiasts about the latest in electronics and emerging technologies.
- FPGAtors is a group of your peers, students who are interested in the same things as you with experience and taken the same classes as you.



MEET THE OFFICERS

FPGAtors



Michael
President



Bo
Vice President



Lucas
Treasurer



Quan
Social Media Coordinator



Nahjay
Secretary



Lathan
Workshop Developer



Miguel
Workshop Developer

ABOUT

Recap on what FPGAtors do!

- Workshops
- Projects
- Resume Review
- Interview Prep



Why do we do workshops?

- To introduce students to FPGAs, RTL development, and the potentials of working with FPGAs.
- To teach students who are interested in learning more about FPGAs and the various topics surrounding it.



What workshops have we done?

- **Completed**
  - **History of FPGAs, FPGA Applications and Workflows by Lathan 9/4/2026**
  - **RTL Fundamentals and Introduction to SystemVerilog by Lathan 9/11/2026**

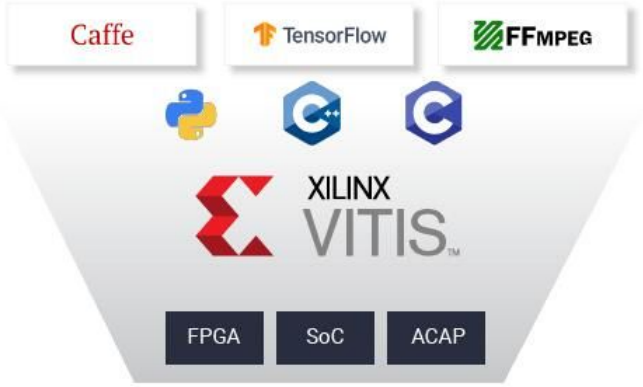
Upcoming Workshops

- Introduction to Verification and Testbenches
- Introduction to UVM
- DSP, Acceleration, & Embedded System Design
- Creating safe clock domain crossings
- PCIE and Communication Protocols
- Computer Architecture
- And more to come!



Next Workshop: Introduction to Vitis (Baby's First Vitis Project)

- When: **October 2nd, 6:00 - 8:00 PM, in LAR234.**
- What:
  - Going over the PS/PL connections and how to set up a PetaLinux environment.
  - Project -> Toggle an LED at 1 Hz, Print "Hello World" at the same time
- Technical Depth: Shallow, come with an open mind on how to use Vitis.
- Collaborative: Not collaborative, but aimed to be reproducible in your own time.
- Goal: Learn something new!





PROJECTS

What projects does FPGAtors have?

Projects are:

- Student-led, voluntary, and open-source
- Require collaboration and serve as a learning experience for all participants

A FEW PROJECTS THIS SEMESTER

Led by Lucas

Guitar Tuner

Intermediate DSP application using Zybo's on-chip SoC and ADC.

Led by Bo

Ethernet

FPGA-Based Ethernet switch. Initial target is an unmanaged 100 Mb Ethernet Switch.

Led by Miguel

RISCV Processor

Beginner project designing and building a RISCV-based processor core.

Project: Guitar Tuner



- Guitar Tuner = Frequency Detector
- Build FFT in HLS and RTL; compare to MATLAB/SciPy
- Determine speedup, trade-offs, and applications.
- Learn how to interface with GPIO on board, SoC & DSP principles, and have fun with RTL design!
- Members Required: Any
- Roles: None
- Goals: Have fun, make something (even if it's bad) and gain a better understanding of FFT
- Hardware: Zedboard || Zybo-Z7-10
- Software: Vitis & Vivado
- Repo: (Will Create by Friday)



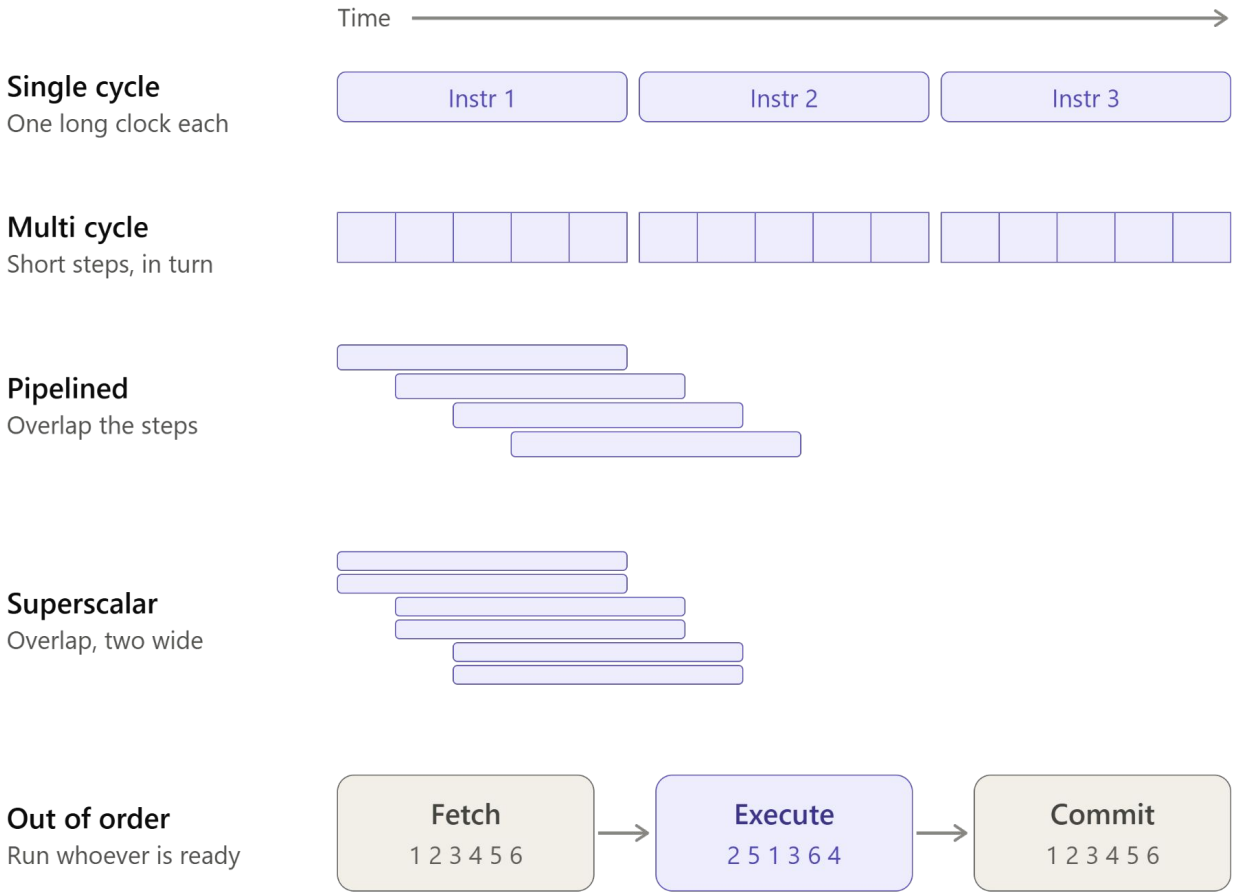


Project: Ethernet

- FPGA Use Case: Networking!
- Basic unmanaged ethernet switch
- Key Components:
  - Softcore (RISCV) Firmware/PHY
  - Ethernet MAC
  - Switching Fabric
  - Discovery Table
- Verification - UVM
  - Design will write plenty of UVM as well!
- Responsible Engineer (RE) for each section
- Project interest form + Design proposal →

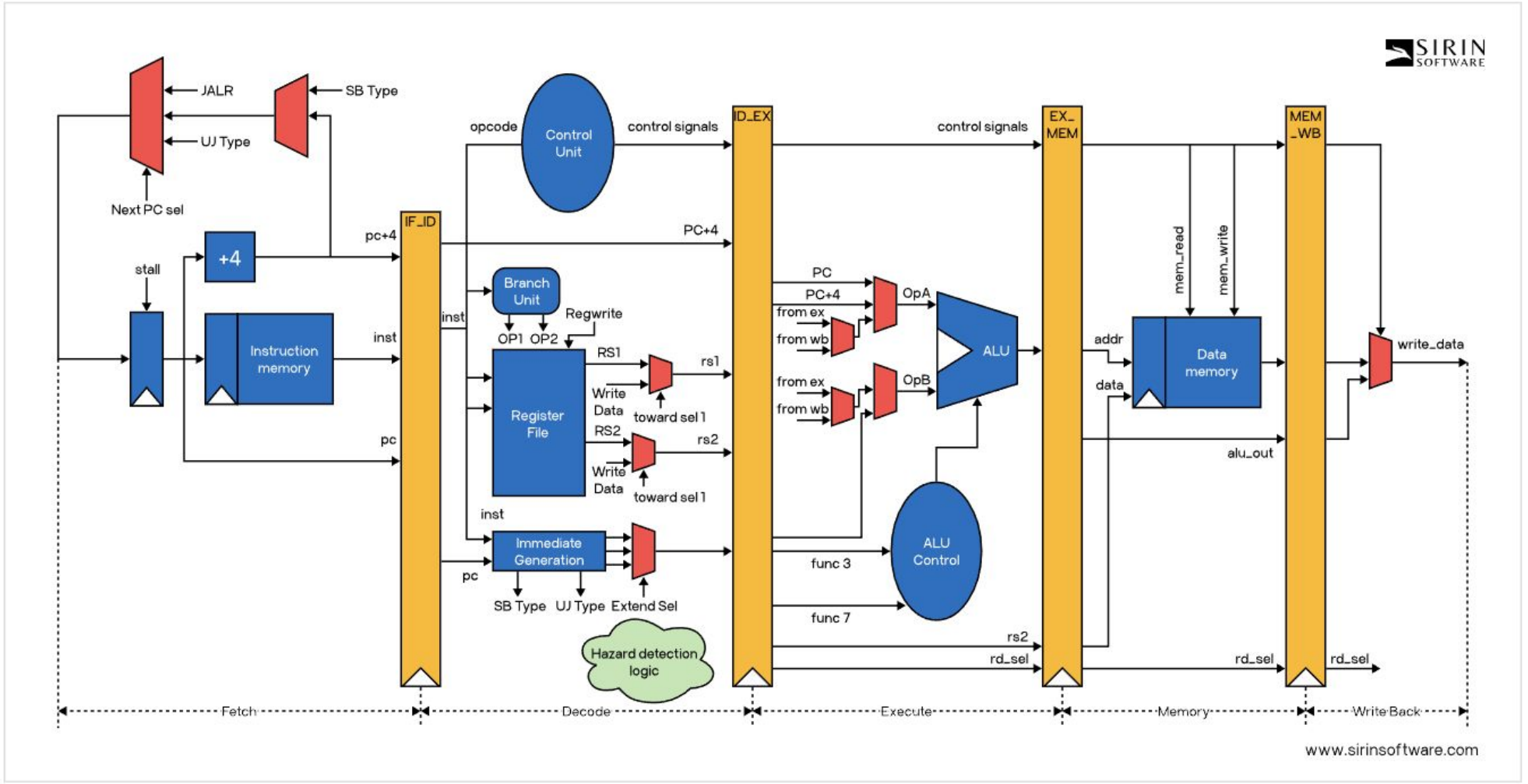


Project: RISC-V Processor



Initial Plan:

- - RV64IM core (64-bit base integer + multiply/divide)
- - Classic 5-stage pipeline (IF, ID, EX, MEM, WB)
- - Weeks 1-2: teach pipelining concepts, then draft the architecture and design plan



Expectations:

- Get ready to grind
- Be prepared to spend weeks learning foundational concepts/skills before we start with real work
- It’s not about where you start, it’s about where you end up!!!!



Do you have your own project idea?

Rent hardware with FPGAtors!



We STILL have

- ZedBoards
- Zybo Z7-10s
- Ultra96 and Ultra96-V2
- Basys3
- AVNet



PARTNERSHIP

We are partnering up with AMD



Thank you!

Questions?

Workshops | Projects | Project Space | AMD Partnership

Scan for attendance

Scan for AMD Survey